Low-Power CMOS Image Sensor Based on Column-Parallel Single-Slope/SAR Quantization Scheme

Fang Tang, *Student Member, IEEE*, Denis Guangyin Chen, *Student Member, IEEE*, Bo Wang, and Amine Bermak, *Fellow, IEEE*

***Abstract*— This paper presents a low-power megapixel image sensor design. In this paper, a column-parallel 11-bit two-step quantization scheme is proposed. It consists of a 3-bit single-slope analog-to-digital converter (ADC) and an 8-bit successive approximation register (SAR) ADC. The power consumption of the column-parallel circuitry is significantly reduced when compared with the traditional single-slope ADC and other low-power ADC schemes because smaller SAR ADC reference voltages are selected after quantizing the first three most significant bits. In addition, as only an 8-bit SAR ADC is required in the proposed quantization scheme, the capacitor array matching can be greatly relaxed compared with an 11-bit SAR ADC thus, resulting in noncalibration feature. A 1200 × 800 pixel resolution color CMOS image sensor (CIS) is fabricated using TSMC 0.18-μm CIS technology. The measurement result shows that the total power consumption figure-of-merit of this research is only 1.33 mW/megapixel/frame under 3.3-V (analog)/1.8-V (digital) power supply.**

***Index Terms*— APS, CMOS image sensor, low power, SAR, single slope.**

I. Introduction

NOWADAYS state-of-the-art image sensors impose great design challenges as ultralow-power design is required to meet requirements for portable consumer electronic market while enabling for high spatial resolution and on-chip digital signal processing [1].

Column-parallel single-slope analog-to-digital converter (ADC) [2] is widely used for the commercial high-resolution CMOS image sensor (CIS) product. The traditional single-slope ADC is, however, not power efficient compared with other ADC schemes, because the quantization period is exponentially increased with the quantization resolution. Typically, for an N-bit resolution, more than 2^N cycles are required. Cyclic ADC (also named as an algorithmic ADC) [3] and successive approximation register (SAR) ADC [4]-based column-parallel quantization circuits are more power efficient than their single-slope counterpart. There are, however, still several drawbacks for the above-mentioned schemes. Cyclic ADC requires very high-performance analog amplifier and good capacitor matching. SAR ADC removes the need for the amplifier, however more accurate matching is required compared with cyclic ADC as the LSB capacitor must be matched with the most significant bit (MSB) capacitor. Therefore, although the SAR-based column-parallel circuit has the best power efficiency, its chip area is very large when considering more than a 10-bit resolution while calibration is normally mandatory [5]. Other column-parallel ADC schemes, such as two-step single-slope ADC [6], [7] and inverter-based sigma delta ADC [8], will require more than 100 cycles to obtain the digital data.

In this paper, we report an image sensor design with a novel two-step column-parallel ADC. The quantization circuit consists of a 3-bit single-slope ADC followed by an 8-bit SAR ADC. The proposed ADC scheme has lower power consumption compared with the traditional one-step or two-step single-slope (TSSS) ADC as well as the cyclic ADC scheme. When compared with an 11-bit SAR ADC, the proposed design does not require any calibration to guarantee the monolithic quantization response, resulting in higher chip area efficiency. The proposed image sensor compares favorably against state-of-the-art designs.

This paper is organized as follows. Section II describes the imager architecture and circuit implementation. Section III describes the measurement results and finally, Section IV summarizes the conclusion.

II. Imager Architecture and Implementation

A. Related Work on Two-Step ADC

The two-step ADC scheme is proposed to address the power consumption issue for the high pixel resolution image sensor. Fig. 1 shows the timing diagrams for the conventional TSSS ADC [6] and the advanced TSSS ADC [7], where Vin represents the pixel output voltage.

The conventional scheme needs to broadcast multiramp voltages into the whole ADC array. The advanced scheme generates the fine ramp with each ADC according to the coarse quantization data. Therefore, a lot of power incurred by multiramp voltage generation can be saved. Although the advanced TSSS ADC only consumes one-quarter of the power compared with the conventional scenario, the quantization cycle for both schemes are still more than 100 clock cycles.

Manuscript received August 26, 2012; revised November 11, 2012, January 12, 2013, March 10, 2013, and May 3, 2013; accepted May 20, 2013. Date of publication June 25, 2013; date of current version July 19, 2013. This work was supported in part by the Hong Kong Research Grant Council under Grant 610412. The review of this paper was arranged by Editor J. R. Tower.

F. Tang is with the Chongqing University, Chongqing 400044, China.

D. G. Chen, B. Wang, and A. Bermak are with the Hong Kong University of Science and Technology, ECE Department, Kowloon 999077, Hong Kong (e-mail: denischn@gmail.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2013.2268207

0018-9383/$31.00 © 2013 IEEE

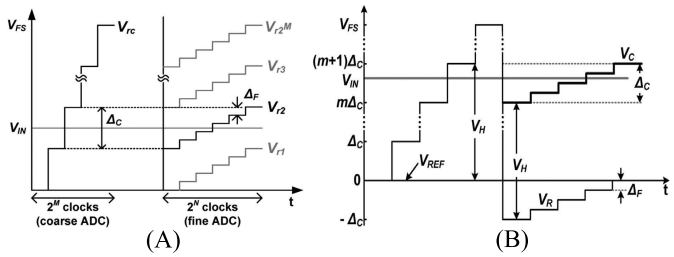


Fig. 1. Timing diagram for the (a) conventional [6] and (b) advanced TSSS ADCs [7].

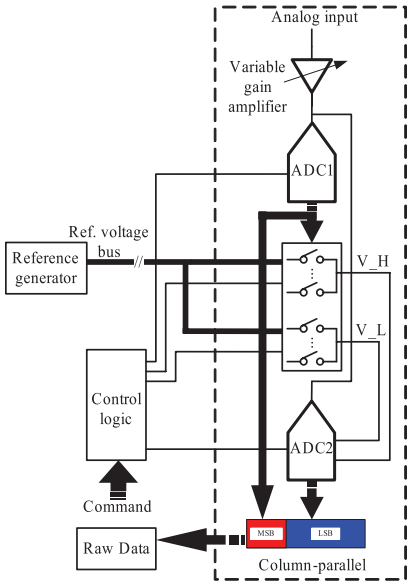


Fig. 2. Block diagram of the column-parallel circuit.

B. Proposed Two-Stage Quantization Principle

To reduce the quantization cycle, we propose a novel two-step quantization topology. In this proposed scheme, the ADC is split into a 3-bit single-slope ADC and an 8-bit SAR ADC, instead of two single-slope stages. The architecture of the proposed column-parallel circuit is shown in Fig. 2.

In the proposed column-parallel circuitry, the pixels' analog output is initially amplified by a variable gain amplifier (VGA). The gain can be tuned from 1× to 8×. The output of the VGA is quantized by a 3-bit single-slope ADC. The number of quantization cycle and the reference voltage is 15 instead of 7, where one redundant bit is required to relax the comparator offset and noise requirement. Without the redundant bits, the comparator offset and noise voltage must be smaller than 0.6 mV for 1.2-V input range. With the redundant bit, the single-slope ADC can tolerate 37.5-mV variation ($\triangle V/2$). The quantized 3-bit digital data from the single-slope ADC determine the voltage subregion V_H and V_L for the subsequent SAR ADC, which are defined as the upper and lower reference voltages, respectively. With one extra cycle between the single-slope and SAR quantization phases, the input signal Vin is sampled in the SAR's capacitor array using bottom plate sampling technique. Then, the SAR ADC quantizes the input voltage Vin within the voltage range $V_H - V_L$ to an 8-bit LSB code. In addition to the one sampling cycle, eight cycles are required for the SAR quantization, which is similar to the conventional SAR operating principle [4]. The transient response of the two-stage quantization scheme is shown in Fig. 3.

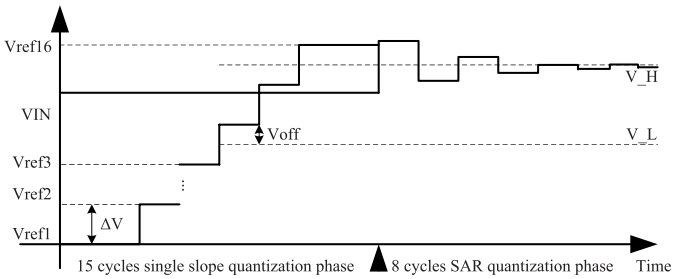


Fig. 3. Transient response of the column-parallel quantization circuitry.

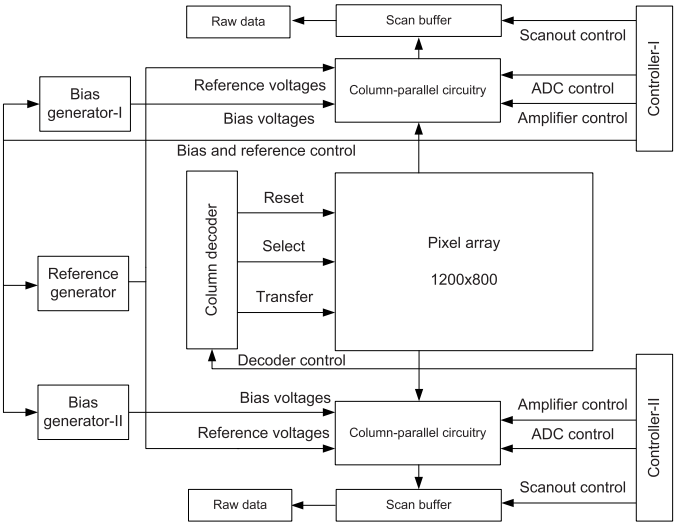


Fig. 4. Architecture of the proposed image sensor.

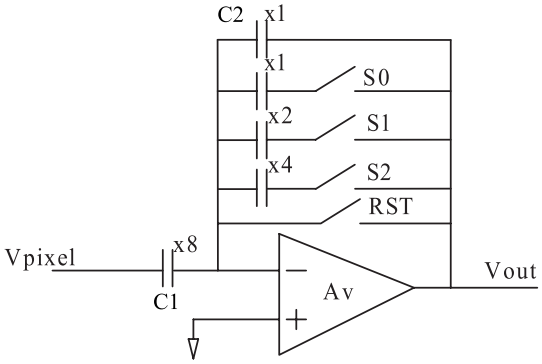


Fig. 5. Schematic view of the VGA.

C. Proposed Image Sensor Implementation

The proposed image sensor top architecture is shown in Fig. 4. This imager consists of 1200 × 800 pixel array, column-parallel circuit, logic controller, reference, and bias voltage generators.

The schematic view of the VGA in the column-parallel circuit is shown in Fig. 5. Compared with the design in [4], the sampling capacitance in Fig. 5 is 8×, instead of 1×, thus the

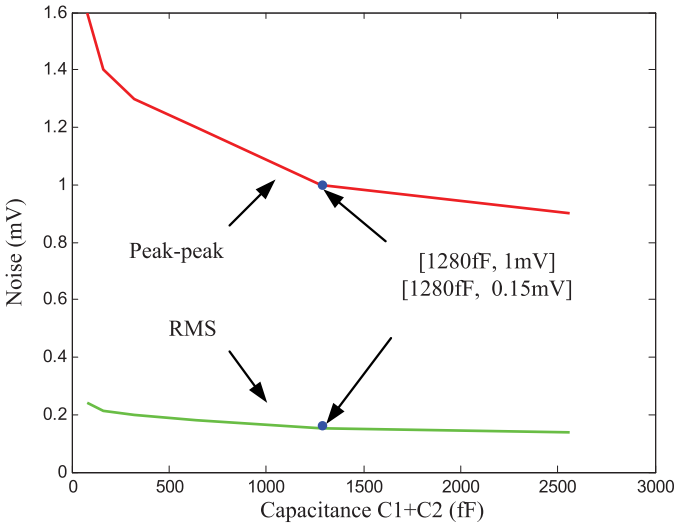


Fig. 6. Estimated overall output random noise as a function of the total capacitance.

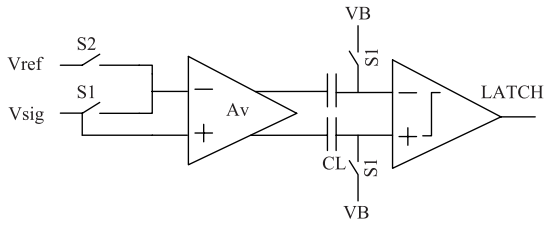


Fig. 7. Topology of the comparator.

total capacitance requirement (sampling capacitor + feedback capacitor) is reduced by half while the KT/C sampling noise for all input range is guaranteed. The total capacitance in the preamplifier is about 1.2 pF. The amplifier transistors are large in size enough to ensure that the output noise is within a 12-bit resolution requirement. The metal-to-metal capacitor array and the transistors share the same chip area, which is about 7 × 250 μm. The overall output noise as a function of the total capacitance is shown in Fig. 6 where the gain D is set to eight.

The open-loop gain A_v must be large enough to minimize the gain variation between columns. The closed-loop gain, G, is expressed as follows:

$$G = \frac{Av}{1 + \frac{Av}{D}} \Rightarrow \frac{\partial G}{\partial Av} = \left(\frac{D}{Av + D}\right)^2 \tag{1}$$

where D is the gain control word (a value between 1 and 8). As $A_v >> D$, 1 can be further derived as 2.

$$\frac{\partial G}{\partial Av} \approx \left(\frac{D}{Av}\right)^2. \tag{2}$$

For example, A_v = 32 dB with 4% variation between two ADC channels and $D = 8$, the closed-loop gain $\triangle G$ is 0.064, which equates to a 0.8% interchannel gain variation. In this design, as the transistor sizes are large, the interchip A_v variation is smaller than 1% according to the Monte Carlo simulation, leading to a $\triangle G$ of 0.2%.

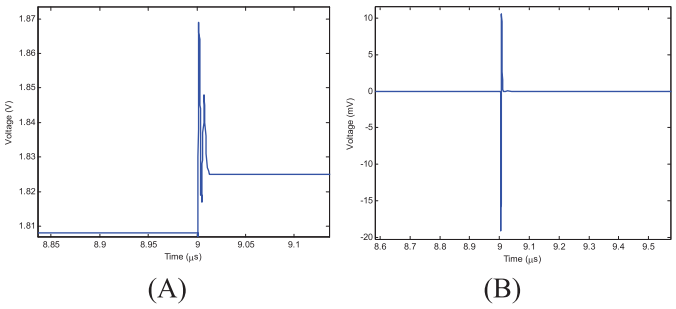


Fig. 8. Simulated (a) single-ended and (b) differential kickback noise on the coupling capacitor.

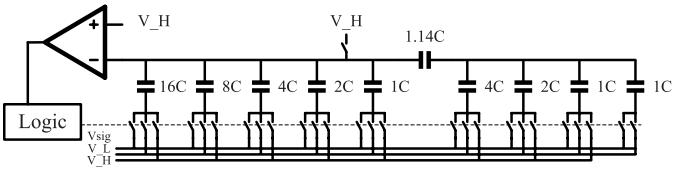


Fig. 9. Topology of the SAR ADC.

The comparator used in both the single-slope ADC and the SAR ADC shares the same topology shown in Fig. 7. The comparator consists of a preamplifier and a latch, with two coupling capacitors. At the beginning of the quantization phase, S1 is closed and the comparator is reset. The input nodes connect to the same voltage and thus, the comparator output offset voltage is stored on the two coupling capacitors CL. In contrast to the design in [2], this topology does not need a feedback, and as the capacitors are located at the output node, the input referred KT/C noise on the capacitor is greatly attenuated by the factor of the amplifier gain. Compared with more than 2-pF total capacitance for the design in [2], this proposed topology shown in Fig. 7 requires only 100 fF for each coupling capacitor, leading to significantly chip area saving. During the quantization phase, S2 is closed and the reference voltage Vref will finally ramp past the signal voltage. Therefore, there is no signal-dependent offset variation at the end of quantization. In addition, the amplifier differential outputs and the inputs of the latch are isolated through the two coupling capacitors, instead of being directly connected. Therefore, the kickback noise from the latch is attenuated by the coupling capacitor. The simulated kickback noise on the two coupling capacitors CL is shown in Fig. 8. When considering gain preamplification of greater than 100, the input refereed kick back noise is smaller than 0.2 mV.

The SAR ADC is implemented based on the split-capacitor topology, which is shown in Fig. 9.

The capacitor array is split into a 5-bit and a 3-bit subarrays. Thus, only 41.14 unit capacitors are required. In addition, during the quantization phase, the maximum equivalent load capacitance observed from V_H and V_L is 32 unit capacitors thus, the power consumption for both the SAR ADC and the reference voltage generator is greatly reduced. According to the Monte Carlo simulation, the matching requirement of the capacitor array can be guaranteed with unit capacitance of 30 fF (5 × 5 μm).

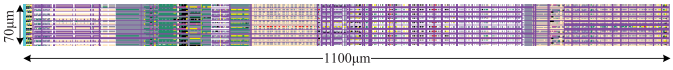


Fig. 10. Overall column-parallel circuit layout.

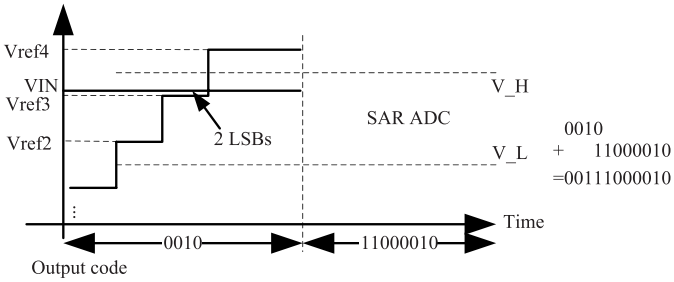
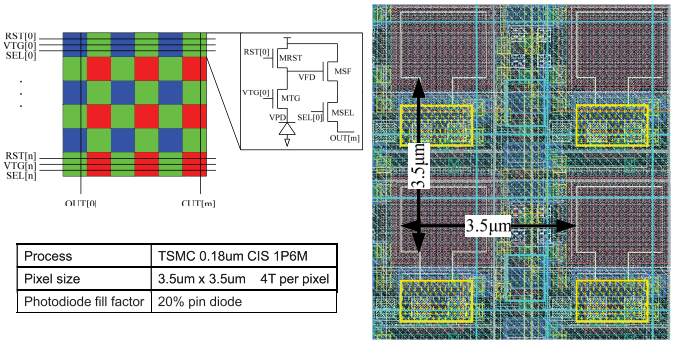


Fig. 11. Error correction algorithm.



Process	TSMC 0.18um CIS 1P6M
Pixel size	3.5um x 3.5um 4T per pixel
Photodiode fill factor	20% pin diode

Fig. 12. Schematic view and layout of the pixel.

In this paper, the read-out circuit is realized using D flip-flop chain. It should be mentioned that although D flip-flop chain offers reliability and IP advantages, the power consumption is much higher than static RAM (SRAM)-based read-out circuitry. In every cycle, all the D flip-flop cells are triggered compared with only one cell enabled for an SRAM implementation. According to the simulation, more than 10 times power is consumed using D flip-flop chain and its peak current is even higher. The overall column-parallel circuit layout is shown in Fig. 10. The chip area is 7 μm $\times$ 1.1 mm. To alleviate the floor-planning constraints with respect to the pixel pitch requirements, two column-parallel banks are implemented on both sides of the pixel array.

The four MSBs from the single-slope ADC and the eight LSBs from the SAR ADC are processed by an error correction algorithm to generate the final digital data. To clearly explain the mechanism, we assume the input voltage Vin is two LSBs higher than Vref3. If the quantization noise of the single-slope ADC is smaller than two LSBs, the 4-bit output digital code of the single-slope ADC will be correctly equal to 0011. Because of quantization noise, the ADC incorrectly, however, generates a 0010 code, as shown in Fig. 11. Without the redundant bit, the reference voltages feeding into the following SAR ADC will be Vref2 and Vref3. Therefore, the input voltage will not be located within these two reference voltages and mission code will occur. In this paper, we use the last MSB from the single-slope ADC as a redundant bit to correct the output data. Still assuming the input voltage with two LSBs higher than Vref3 and the output code of the single-slope ADC is incorrectly equal to 0010 because of the noise, V_H and V_L will feed into the following SAR ADC instead of Vref2 and Vref3. As $V_H - V_L = 2$(Vref3–Vref2), only three effective bits are obtained by the single-slope ADC. After the 8-bit SAR quantization, the LSB output code will be 11000010 and the final 11-bit output is recombined as 00111000010, as shown in Fig. 11.

The pixel is implemented using the standard 4-T pinned diode active pixel sensor structure provided by the TSMC CIS process. Bayer pattern is used to realize the color filter. The schematic view and layout of the pixel are shown in Fig. 12. The pixel pitch is mainly limited by the minimum size of transistor MTG, which is 1.06/0.7 μm. The MRST transistor has a negative threshold voltage to reset the floating node to the supply voltage.

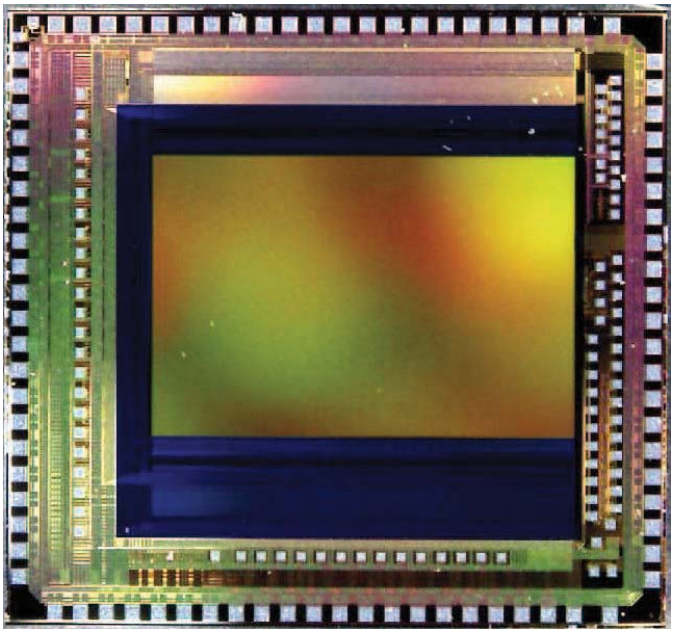


Fig. 13. Chip microphotograph.

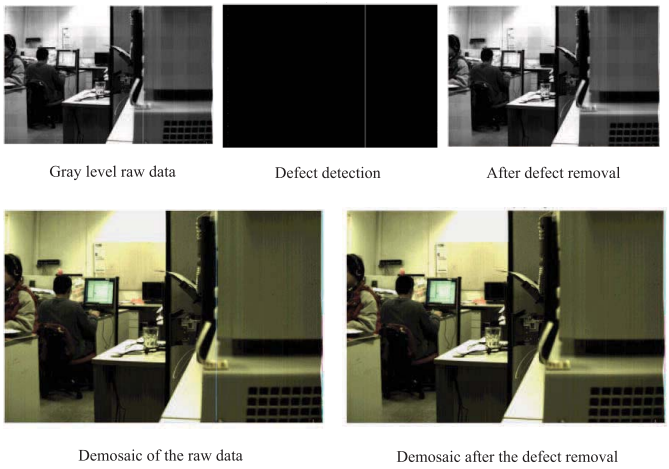


Fig. 14. Sample image before and after defect removal.

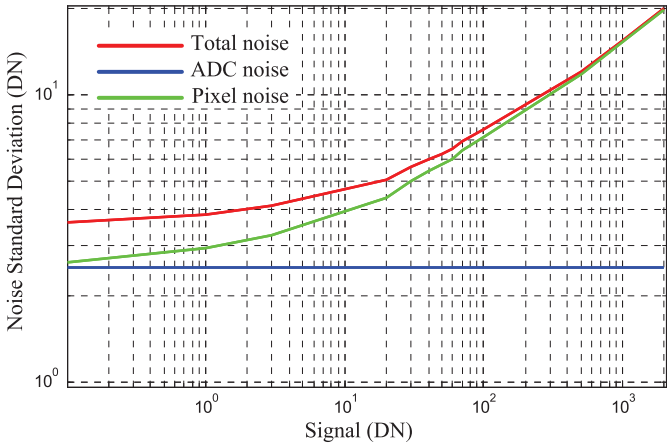


Fig. 15. Photon transfer curve.

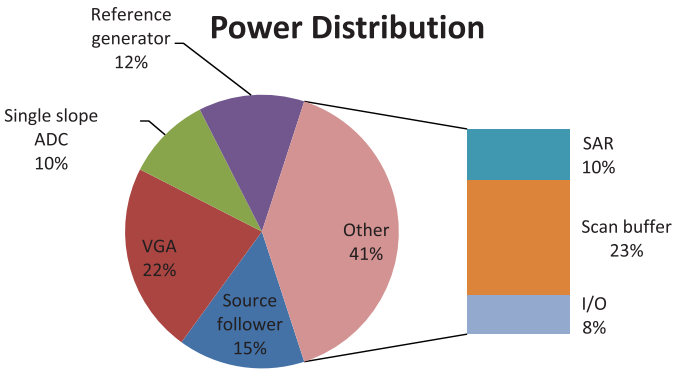


Fig. 16. Power consumption distribution for each building block.

III. Experimental Results

The proposed 1200 × 800 pixel resolution color CIS chip is fabricated using TSMC 0.18-μm CIS process. The chip microphotograph is shown in Fig. 13. The chip size is 6 × 6 mm. The sample images are shown in Fig. 14. Defects in pixel and column circuit are detected and removed by off-chip signal processing. The final color image is produced by a MATLAB proprietary demosaic algorithm.

A linear well capacity (LWC) of 17 ke^- is measured with about 0.6-V output voltage swing. The photo current/pixel is 57.3 pA under 25 000-lux (lx) light intensity. The conversion gain is estimated as follows:

$$CG = \frac{\Delta V_O}{LWC} \approx 35\mu V/e^- \tag{3}$$

where $\Delta V_O = 0.6V$ is the linear pixel output voltage swing. The measured output digital code from the ADC shows about 2.5-LSBs noise floor in dark (1.5 m$V_{\rm rms}$). The pixel transient output response shows a 9.7-ke^-/lx. sec pixel sensitivity. The dark current of the entire pixel array is 15 pA, leading to an average of 100-e^-/s dark current for each pixel. The ADC's dynamic range is defined as the ratio between the well capacity and the noise floor in dark. According to (4), the ADC dynamic range is about 58.3 dB, for 1.2-V input range. The peak SNR is about 40 dB because the temporal noise increases to about 20 $DN_{\rm rms}$ (1%) when the pixel output reaches the maximum value. The photon transfer curve of the pixel is shown in Fig. 15, which shows a 3.5-LSBs (DN) total noise. Thus, the imager dynamic range is about 55 dB. The pixel noise consists of the photo shot noise, thermal noise, and flicker noise of the source follower transistor, and so on. When the light intensity is large, photo noise dominates the pixel noise whereas source follower transistor noise dominates in dark. Therefore, the pixel noise in dark is larger than zero (about 2.5 DN in this paper)

$$DR = 20\lg\frac{2042DN}{2.5DN} \approx 58.3 \text{ dB}. \tag{4}$$

The power consumption of the proposed image sensor chip is about 40 mW at a frame rate of 35 frames/s. The power consumption distribution for each building block is shown in

TABLE I
Performance Summary of the Proposed Design

Process	TSMC 0.18um CIS 1P6M 3.3V(Analog, I/O) 1.8V(Digital)
Pixel resolution	1200H x 800V
Pixel size	3.5um x 3.5um 4T per pixel
Photodiode fill factor	20%
Imaging area	4.2mm x 3mm
Total chip size	6mm x 6mm
ADC resolution	11 bit
Frame rate	35frames per second (full resolution)
RGB filter	Bayer pattern
Averaged power	40mW
Peak current	Estimated 225mA
On chip analog pre-amplification	x1-8
Linear Well capacity	17ke$^-$
Conversion gain	35μV/e$^-$
Sensitivity	9.7ke$^-$/lux.s
ADC Temporal noise in dark	1.5mVrms or 2.5LSBs or 0.15%
ADC resolution	11-bit
PRNU	0.5%
ADC Column FPN	2 LSBs or 1.2mV or 0.1%
ADC DNL	+1.65LSB/-1.45LSB
Master clock frequency	40MHz
VGA gain variation	0.5%
ADC dynamic range	58.3dB
Total dynamic range	55dB
Peak SNR	40dB
Optical format	1/4-inch

TABLE II
Summarized Comparison With Other Types of Column-Parallel Architectures

Architecture	Single Slope	Cyclic	SAR	Two stages SS	Sigma delta	This work
Power consumption (mW/Mpixels .frame/s)	3.75 [2]	1 [3]	2 [4]	0.7[7]	0.7[8]	1.33 0.8 using SRAM & w/o VGA
Cycles /sample	>1000	12	12	>100	120	24
Main design requirement	PLL	Amplifier performance	12bit cap array	Error correction	Supply & switch noise	Variable gain amplifier 3bit SSADC+8bit SAR
Technology	0.18μm 1P3M	0.25μm CIS 0.18μm CIS	0.18μm 2P3M	0.35μm	0.13μm	0.18μm CIS
Pixel resolution	6.4M	0.26M/0.3M	8.9M	0.076M	2.1M	0.96M
Conversion Time	7.2μs	500ns	1.7μs	4μs	2.3μs	12μs

Fig. 16. Almost 45% power is consumed by the VGA and the read-out scan buffer. If there is no preamplification requirement and the scan buffer is replaced by SRAM, only about 25 mW is needed to operate the proposed image sensor, which amounts to only 0.75 mW/megapixel/frame. The performance of the proposed CIS is listed in Table I and the comparison with the other types of column-parallel architectures is listed in Table II.

IV. Conclusion

In this paper, a low-power 1200 $\times$ 800 image sensor was fabricated and measured. The column-parallel quantization circuit was implemented using a 3-bit single-slope ADC and an 8-bit SAR ADC. A redundant bit was inserted into the single-slope quantization to relax the offset requirement of the comparator. Noncalibration and moderate chip area were simultaneously achieved for the proposed quantization circuitry with a standard 8-bit split-capacitor SAR ADC. The chip was fabricated using TSMC 0.18-μm CIS process, with a 6 $\times$ 6 mm chip area. Measurement results showed that the total power consumption of the whole chip is 45 mW at 35 frames/s, which amounts to a 1.33-mW/megapixel/frame figure-of-merit. The chip area of the column-parallel circuit cell was 7 μm $\times$ 1100 μm, including preamplifier, ADC, and scan buffer.

References

[1] K. Kagawa, S. Shishido, M. Nunoshita, J. Ohta, "A 3.6 pW/frame·pixel 1.35 V PWM CMOS image with dynamic pixel readout and no static bias current," in *Proc. IEEE ISSCC*, Feb. 2008, pp. 54–595.

[2] S. Yoshihara, Y. Nitta, M. Kikuchi, K. Koseki, Y. Ito, Y. Inada, S. Kuramochi, H. Wakabayashi, M. Okano, H. Kuriyama, J. Inutsuka, A. Tajima, T. Nakajima, Y. Kudoh, F. Koga, Y. Kasagi, S. Watanabe, and T. Nomoto, "A 1/1.8-inch 6.4 MPixel 60 frames/s CMOS image sensor with seamless mode change," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2998–3006, Dec. 2006.

[3] M. Furuta, Y. Nishikawa, T. Inoue, and S. Kawahito, "A high-speed, high-sensitivity digital CMOS image sensor with a global shutter and 12-bit column-parallel cyclic A/D converters," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 766–774, Apr. 2007.

[4] S. Matsuo, T. J. Bales, M. Shoda, S. Osawa, K. Kawamura, A. Andersson, M. Haque, H. Honda, B. Almond, Y. Mo, J. Gleason, T. Chow, and I. Takayanagi, "8.9-Megapixel video image sensor with 14-b column-parallel SA-ADC," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2380–2389, Nov. 2009.

[5] R. Xu, B. Liu, J. Yuan, "A 1500 fps highly sensitive 256 $\times$ 256 CMOS imaging sensor with in-pixel calibration," *IEEE Trans. Electron Devices*, vol. 47, no. 6, pp. 1408–1418, Jun. 2012.

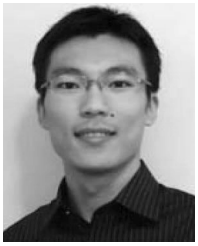
[6] M. F. Snoeij, P. Donegan, A. J. P. Theuwissen, K. A. A. Makinwa, and J. H. Huijsing, "Multiple-ramp column-parallel ADC architectures for CMOS image sensors," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2968–2976, Dec. 2007.

[7] S. Lim, J. Lee, D. Kim, and G. Han, "A high-speed CMOS image sensor with column-parallel two-step single-slope ADCs," *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 393–398, Mar. 2009.

[8] Y. Chae, J. Cheon, S. Lim, M. Kwon, K. Yoo, W. Jung, D.-H. Lee, S. Ham, and G. Han, "A 2.1 M pixels, 120 frame/s CMOS image sensor with column-parallel $\Delta\Sigma$ ADC architecture," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 236–247, Jan. 2011.

Fang Tang (S'07) received the Ph.D. degree from the Hong Kong University of Science and Technology, Hong Kong, in 2013.

His current research interests include mixed-signal circuit design for low-power and high-speed CMOS image sensors and ADCs.



Denis Guangyin Chen (S'07) is currently pursuing the Ph.D. degree with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong.

He is a member of the Smart Sensory Integrated System Laboratory.

Bo Wang is currently pursuing the Ph.D. degree with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong.

His current research interests include smart CMOS temperature sensors and sensor interfaces.

Amine Bermak (M'99–SM'04–F'12) received the Ph.D. degree in electronic engineering from Paul Sabatier University, Toulouse, France, in 1998.

He is currently a Professor in the Electronic and Computer Engineering Department, Hong Kong University of Science and Technology, Hong Kong.